Full-Swing Complementary BiCMOS Logic Circuits

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ABSTRACT

Full-swing BiCMOS logic circuits for complementary MOS/bipolar technologies are described. The circuits utilize a complementary emitter-follower driver configuration for efficient driving, switched base-emitter shunting to achieve full swing, and CMOS diodes for base-to-base clamping. The performance of the circuits has been demonstrated in a BiCMOS technology featuring 0.8 μm design rules and a single-poly (poly-emitter) npn-BJT with a f_T of 15 GHz. Using an n-well-base, substrate pnp-BJT ($f_T \simeq 500$ MHz), a gate delay (fan-in = 2, fan-out = 1) of 232 ps was obtained with a 3.6 V supply. Also low voltage operation has been demonstrated down to 1.4 V.

I. INTRODUCTION

The potential of BiCMOS technologies has been successfully demonstrated in various BiCMOS circuits including static RAMs [1], microprocessors [2], and gate arrays [3,4]. However, in gate array applications, there are growing concerns about the leverage of conventional BiCMOS logic circuits over pure CMOS as the power supply is reduced in scaled technologies.

The major reasons why conventional BiCMOS circuits quickly lose their performance leverage over CMOS as the supply voltage is lowered are because, as shown in Figure 1, they utilize the gated-diode driver for pull-down and have a partial logic swing (from V_{BE} to $V_{DD}-V_{BE}$). Since maximum base current for the pull-down BJT is roughly proportional to $V_{DD}-2V_{BE}-V_T$, where V_T is the threshold voltage of n-MOSFET with a substrate bias of V_{BE}, the pull-down speed degrades quite rapidly with V_{DD} scaling and the circuit stops operation if V_{DD} is below $2V_{BE}+V_T$.

To improve the leverage and scalability of BiCMOS, new circuits with proper driver configurations that have better base drive for output BJTs are needed. This paper describes two high-speed, full-swing BiCMOS logic circuits for complementary MOS/bipolar technologies. These advanced circuits feature push-pull emitter-follower drivers, controlled base-emitter shunting circuitry using MOSFETs, and CMOS diodes for base-to-base clamping. For scaled BiCMOS logic circuits with reduced power supply voltages, the emitter-follower driver configuration and the full-swing techniques with base-emitter shunting have been shown to be most advantageous for enhancing the performance [5].

II. CIRCUIT DETAILS

Figures 2 and 3 show the details of the full-swing complementary MOS/bipolar logic (FS-CMBL) 2-input NAND circuits. Both circuits implement the logic in the CMOS circuitry (MN1, MN2, MP1, and MP2) and drive the output through the push-pull emitter-follower (QN1 and QP1). To ensure that only one BJT is active at any time, the two base nodes of the emitter-follower are clamped using the CMOS diode (the MN4-MP4 pair). For proper clamping, the MOSFET threshold voltages (V_{Tn} and V_{Tp}) need to be smaller than the BJT turn-on voltage (V_{BE}). This CMOS diode consumes less area and adds less parasitic capacitance onto the nodes X and Y than a BJT diode.

A. FS-CMBL Circuit without Feedback

The circuit in Figure 2 achieves full swing through the base-emitter shunting MOSFETs MN3 and MP3. The gate of the n-channel MOSFET MN3 is connected to V_{DD} and that of the p-channel MOSFET MP3 is tied to V_{SS} or GND. In an initial state where both inputs (A and B) are '1', Y is fully discharged to GND. Thus, without MN3, the output node O would stay at V_{BE}. However, with MN3, Y and O are shorted through MN3. Therefore, the output is pulled to GND and QP1 becomes firmly OFF. The node X is held at V_{Tn0} by MN4 and QN1 is cut off. Here V_{Tn0} is the n-MOSFET threshold voltage with zero back bias. Because MP3 and MP4 have a large substrate bias ($= V_{DD}-V_{Tn0}$), the body effect results in $|V_{Tp}|$ being greater than V_{Tn0} and MP3 and MP4 are OFF.

If A is changed to '0', MP2 begins to source a current and charge X up. Because MP3 remains OFF until X reaches $|V_{Tp}|$, most of the current flows into the base of QN1. This turns QN1 on and a large emitter current pulls up the output. A part of the current from MP2 also charges Y up through the diode MN4. For this transient, QP1 is held OFF strongly because MN3 is ON in addition to the diode clamp between X and Y, as long as the output is lower than $V_{DD}-V_{Tn}$.

When X rises above $|V_{Tp}|$, MP3 becomes ON and bypasses a fraction of the base current to the output. To prevent premature cut-off of QN1 before X reaches V_{DD}, MP3 should be made weak. MN3 will be OFF if both O and Y get higher than $V_{DD}-V_{Tn}$. Finally, when X reaches V_{DD}, the threshold voltages of MP3 and MP4 return to V_{Tp0} and MP3 pulls up the output to V_{DD} by discharging the base-emitter junction of QN1. The diode MP4 now clamps Y at $V_{DD}-|V_{Tp0}|$ and prevents QP1 from turning on. If A is changed back to '1', the opposite transition occurs with complementary circuit operation.

A minor drawback of this circuit is that MP3 (or MN3) starts to turn on as soon as the gate-source voltage is greater than V_{Tp} (or V_{Tn}) during pull-up (or pull-down). Although the body effect is large for modern technologies, these threshold voltages are only about 1.5 V when V_{DD} = 5 V. This results in a premature bypass of the base drive current and, consequently, a slower speed.

B. FS-CMBL Circuit with Feedback

Figure 3 shows an improved FS-CMBL circuit that uses positive feedback to enhance the speed. The circuit is similar to the one in Figure 2 except that the gates of MN3 and MP3 are driven by the CMOS inverter (MN5-MP5 pair) that inverts the output signal. The function of this inverter is to delay the turn-on of MP3 (or MN3) during pull-up (or pull-down) until the output changes its logical state.

In an initial state where both inputs (A and B) are '1', Y is fully discharged to GND and, if MN3 were OFF, the output O would stay at V_{BE}. However, since this level is lower than the logic threshold voltage of the CMOS inverter (~ half V_{DD}), the node Z is high and MN3 is fully ON. Thus, O is shorted to GND and QP1 is OFF. MN4 holds X at V_{Tn0} and QN1 in the OFF state. MP4 is OFF due to the body effect and MP3 is OFF mainly because its gate potential is V_{DD}.

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When A falls to '0', a current will flow through MP2 and charge up the node X. Because MP3 remains OFF until Z falls to $V_X - |V_{Tp}|$, most of the current flows into the base of QN1, turning it on. The output is then pulled up by a large current from QN1. A part of the MP2 current also charges Y up through the diode MN4. Because MP3 is OFF and MN3 is ON (holding QP1 OFF) before the output crosses the inverter logic threshold, the output transient benefits from a full base drive and zero crossover current.

When O rises above the logic threshold voltage, Z falls to GND and MN3 will be OFF immediately. However QP1 will remain OFF through the diode clamp between X and Y. At this point, since V_X ($= V_O + V_{BE}$) is greater than $|V_{Tp}|$, MP3 becomes ON and begins to bypass a fraction of the base current for QN1. Although this causes the final transient to be slower, because the output has already changed its logical state, the circuit speed will not be degraded. MP3 must be optimized to prevent a premature cut-off of QN1 before X reaches V_{DD}. Finally when $V_X = V_{DD}$, the threshold voltages of MP3 and MP4 return to V_{Tp0}. Then MP3 strongly pulls up the output to V_{DD}, discharging the base-emitter junction of QN1 and holding QN1 in the OFF state. The diode MP4 clamps V_{XY} at $|V_{Tp0}|$ preventing QP1 from turning on. If A is changed back to '1', the circuit operates in a complementary way.

This circuit performs better than the circuit in Figure 2 because of the latency in shunting provided through the feedback inverter. The propagation delay of the inverter will add to this latency.

Because the output of this circuit reaches the full supply levels after the feedback inverter changes its logic state, the minimum operation voltage of this circuit is $2V_{BE}$ when the logic threshold voltage is half V_{DD}.

III. EXPERIMENTAL RESULTS

The FS-CMBL circuits have been implemented with a 0.8 μm design rule, npn-only BiCMOS technology [6]. For the pnp devices, n-well-base lateral pnp-BJTs or substrate pnp-BJTs were utilized. The base width of the lateral pnp is defined by the field-oxide to be 0.8 μm (on the mask). For the substrate pnp, the difference between the p+ junction and well depth determines the base width as 0.95 μm. The cut-off frequency of the single-poly, poly-emitter npn-BJT is 15 GHz and that of the substrate pnp-BJT is estimated to be about 500 MHz. Table 1 summarizes the key parameters of the technology.

The circuit in Figure 2 was designed using the lateral pnp and two versions of the circuit in Figure 3 were fabricated, one using the substrate pnp, the other using the lateral pnp. The gate width of each MOSFET used for the logic function (MN1, MN2, MP1, and MP2) is 20 μm, and the emitter sizes of the npn and the pnp are 8 μm x 0.8 μm and 10 μm x 2.4 μm, respectively. Figure 4 shows the SEM micrograph of the FS-CMBL circuit with feedback using the substrate pnp.

The gate delays (fan-in = 2, fan-out = 1) were measured from 19-stage ring-oscillator circuits without and with an additional loading of 15 gates ($\simeq$ 1.6 pF), and are summarized in Figure 5 for 3.6 V operation at room temperature. Despite the poor pnp characteristics and high MOSFET threshold voltages, the unloaded delay of the circuit with feedback using the substrate pnp is 232 ps and the loaded delay is 526 ps. The power dissipation for the unloaded case is 625 μW at 114 MHz. As can be seen, the circuit with feedback is faster than the one without feedback. This proves the effectiveness of the feedback mechanism that controls the base-emitter shunt timing. The two curves for the circuit with feedback also suggest that the substrate pnp is better than the lateral pnp.

The measured gate delay of the FS-CMBL circuit with the substrate pnp is compared with the measured delays of the pure CMOS (gate width = 40 μm) and conventional BiCMOS circuits in Figure 6. Although the pnp-BJT used is poor, the FS-CMBL circuit shows a better driving capability than CMOS and is faster if the load capacitance is larger than about 0.3 pF. It is also slightly faster than the conventional BiCMOS for loads below about 0.5 pF and has comparable driving capability. If a better pnp (e.g., f_T = 8 GHz) is available, the delay and drive capability of the FS-CMBL circuit would improve to 172 ps (unloaded) and 70 ps/pF, respectively, as shown by the dashed line in Figure 6 from the simulation.

The internal waveform of the ring oscillator shown in Figure 7 for the unloaded circuit with the substrate pnp verifies that the circuit achieves a full swing. The advantage of the FS-CMBL circuit over conventional BiCMOS has been demonstrated by operating the circuits with reduced power supply voltages as shown in Figure 8 for the unloaded case. As expected, the FS-CMBL circuit operates for power supplies down to 1.4 V while the conventional partial-swing BiCMOS circuit only functions down to 2.2 V.

IV. CONCLUSION

New full-swing complementary MOS/bipolar logic (FS-CMBL) circuits have been described and shown to be advantageous for reduced power supply applications. These circuits improve speed and power consumption by minimizing the bypass and crossover current during the output transients using the switched, CMOS, base-emitter shunt circuitry. The operation of the FS-CMBL circuits has been successfully demonstrated using a 0.8 μm BiCMOS technology with a 15-GHz npn-BJT. Although the circuits utilize parasitic pnp-BJTs that are slow, the gate delay and driving capability are better than pure CMOS and comparable to the conventional BiCMOS circuit at 3.6 V. The performance leverage will increase with a better pnp-BJT. The circuits function well for power supply voltages as low as 1.4 V and clearly demonstrates the advantages of full swing.

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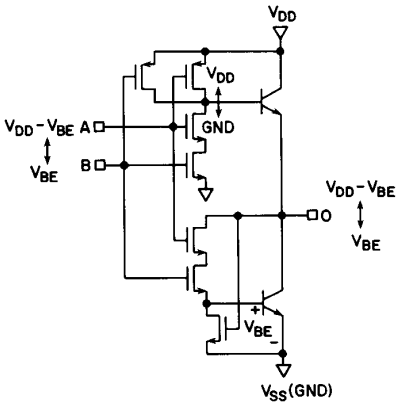

Figure 1. Conventional BiCMOS logic circuit with emitter-follower pull-up and gated-diode pull-down circuitry.

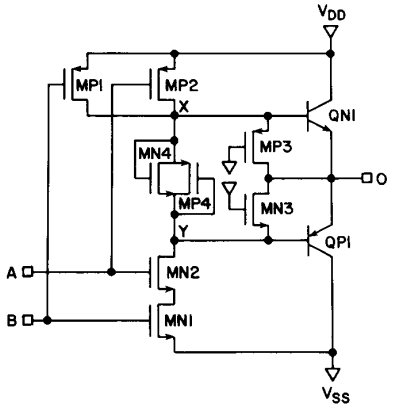

Figure 2. Full-swing complementary MOS/bipolar logic (FS-CMBL) 2-input NAND circuit without feedback.

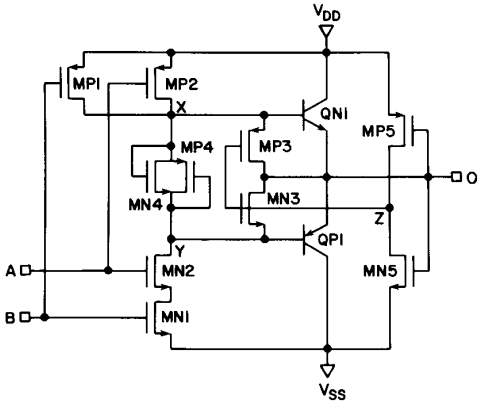

Figure 3. FS-CMBL 2-input NAND circuit with feedback.

MOSFET Threshold Voltages	0.8 / -0.7 V.
MOSFET Channel Lengths	0.6 / 0.6 μm.
BJT f_T's (npn/Substrate-pnp)	15 / $\approx$0.5 GHz

Table 1. Key BiCMOS technology parameters.

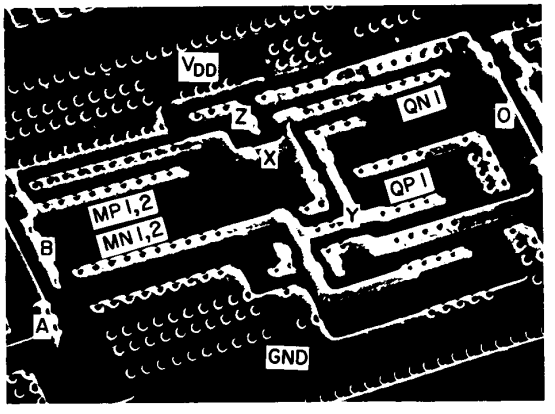

Figure 4. SEM micrograph of the circuit with feedback using the substrate pnp-BJT.

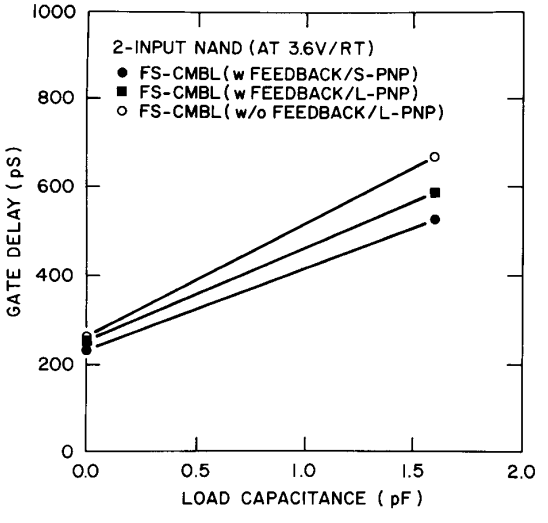

Figure 5. Measured gate delay versus additional load capacitance for the FS-CMBL circuits.

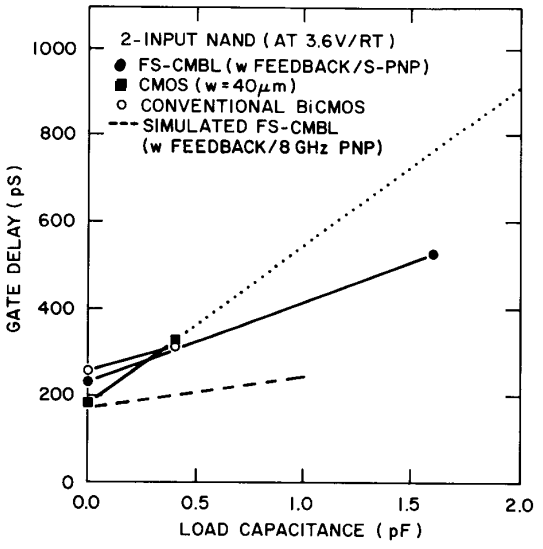

Figure 6. Measured delay comparison between the FS-CMBL circuit with feedback using the substrate pnp and the pure CMOS and conventional BiCMOS circuits for additional load capacitance.

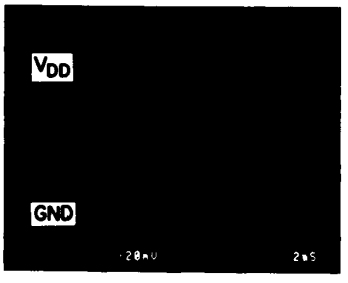

Figure 7. Ring-oscillator waveform of the unloaded FS-CMBL circuit with feedback using the substrate pnp, measured inside the ring (V_{DD} = 3.6 V).

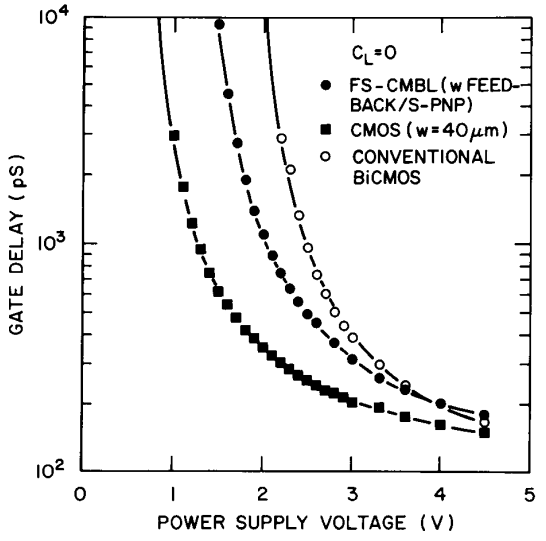

Figure 8. Measured unloaded-delay comparison (versus power supply voltage) between the FS-CMBL circuit with feedback using the substrate pnp and the pure CMOS and conventional BiCMOS circuits.