MULTI-EMITTER BiCMOS Logic circuit family

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ABSTRACT :
In a 64 bit carry look ahead Adder, the use of conventional half micron BiCMOS circuits under 3.6V power supply gives 40% faster delay than the CMOS design. A substantial 85% is obtained with the new Multi-Emitter BiCMOS circuit. A complete logic circuit family with the Multi-Emitter concept is described with a maximum benefit on gates with high number of inputs.

- TECHNOLOGY

To demonstrate the benefits of the Multi-Emitter approach, the BiCMOS circuits are built in a technology derived from a CMOS technology [2] [3], utilizing an N-well process, and an N+ doped polysilicon gate. The channel lengths of NFET and PFET devices are 0.5 micrometer with a DILDD structure to reduce punch through and hot electron effects. The technology features a 9 GHz Ft bipolar NPN .

- BICMOS CIRCUIT PERFORMANCE

As the the BiCMOS technology is improved, the power supply must be reduced to 3.6V with half micron channel length FETs to reduce voltage stress and to limit the power dissipation. A conventional BiCMOS circuit with 30 um width NFET,PFETs has a nominal gate delay of 250ps, Fig 2. For loads above 1 pF the BiCMOS circuit can be 2 times faster than the CMOS.
This is obtained at a 150uW power dissipation, a 12ns Cycle time and a switching factor of 30%.

- BENEFITS OF THE MULTI-EMITTER APPROACH

The basic idea for the Multi-Emitter (ME) approach [1] is shown on fig 1b. It has been observed that, in conventional BiCMOS circuits that use reasonably fast NPN's, the bottom part of the circuit switches faster that the top part. This is because the bottom NPN transistor requires only a few hundred millivolts on its base node to be strongly driven and can therefore be switched ON and OFF very fast. On the opposite, the top part of the circuit is comparatively slower because the base of the bipolar emitter-follower transistor is driven by a CMOS NAND gate, the speed of which depends on the number of inputs : the larger the number of inputs, the slower the gate. As a consequence, the slower part not only imposes its low speed to the circuit but also creates huge crossover current spikes through the top and bottom NPN's that are simultaneously turned on for some period of time.

The novelty of the Multi-emitter circuit consists in replacing the slow CMOS NAND gate with multiple INVERTERS and doing the logic function by OR DOTTING their outputs with multiple emitter-followers. In other words, the parasitic capacitance produced by the logic connection of several devices is moved from the very sensitive CMOS part to the less sensitive bipolar part. Practically the output node capacitance increase due to the emitter dotting is negligible not only because this node is driven very strongly by the bipolar transistors but also because this node already has a large capacitance due to wiring and fan out loading. The net gain is that the upper part of a NAND gate now switches as fast as the upper part of and INVERT circuit, Fig 3.

The result is a better speed and a smaller power dissipation than conventional BiCMOS. The larger the number of inputs, the larger the benefit is, with 15% for a 2 input NAND up to 35% with 4 inputs. It has been verified that the circuit is always faster and dissipates less than the CMOS circuit in same technology. Comparative delay vs load capacitance curves are drawn on fig.2.

- TECHNOLOGY REQUIREMENTS

The Emitter DOT logic implies that the bipolar device can stand the reverse base-emitter voltage imposed by the input inverters with no degradation. A simple reference voltage generator - diode, as shown on fig.1b - allows to reduce that voltage to an acceptable value.

The total gate area is slightly larger than with conventional BiCMOS but signal levels are compatible. The Muti-emitter concept can eventually be restricted to critical paths and mixed with standard BiCMOS in complex chips.

- MULTI-EMITTER CIRCUIT FAMILY

A complete logic circuit family can be built with the ME approach, decomposing the logic into "ORed" blocks. An example is given on Fig.4 where a 2 way XOR Not is designed with a ME 2 way NAND followed by a 2x2 AOI in such way that only inverters are in the critical path.

- APPLICATION : 64 bits ADDER with carry look ahead Multi Emitter circuits give a high performance improvement if it is applied to a 64 bit adder with carry look ahead. The logic for the carry calculation is built from basic blocks of 4 bits with Group Generate and Group Propagate terms. The use of regular BiCMOS in the carry propagation gives a 40 % improvement over CMOS. Up to 85% improvement is obtained in a multi-emitter implementation because it allows an extensive use of 4 Way NAND's.

- GATE ARRAY :

Fig 6 and 7 show two transistor arrangements in a gate array structure. Fig 6 is a Multiplier macro that includes a full adder and Fig 7 shows a microphotograph of two BiCMOS ring oscillators designed for speed comparison.

- CONCLUSION

In an half micron BiCMOS technology it has been demonstrated that a novel approach in BiCMOS logic circuit named Multi-Emitter has outperformed the known BiCMOS circuit as the CMOS at low loading.

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[3] S.Ogura et al, "A Half Micron Mosfet Using Double Implanted LDD" , IEEE Proc. IEDM dec 1982
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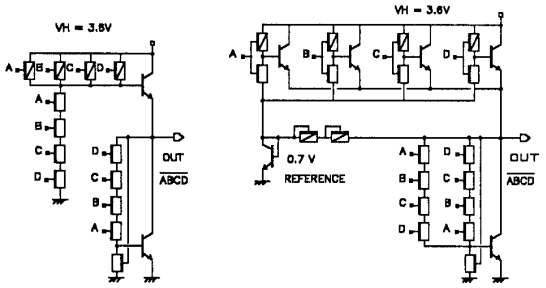
TABLE I		
PARAMETERS	NOMINAL VALUES	
Channel Length	(NFET)	: 0.50 um
	(PFET)	: 0.50 um
Gate Oxide Thickness		: 14.0 nm
Device Vt.	(NFET)	: 0.5 Volts
	(PFET)	: -1.0 Volts
Saturation Transconductance	(NFET)	: 125 mA/V/mm
	(PFET)	: 75 mA/V/mm
NPN Ft		: 9.0 GHz
NPN Beta		: 90
N-Well / Substrate Voltage		: 3.6 / 0 Volts
Minimum Contact		: 1 x 1 um



(a) Conventional (b) proposed Multi-Emitter

Figure 1 : 4 way NAND BiCMOS CIRCUITS

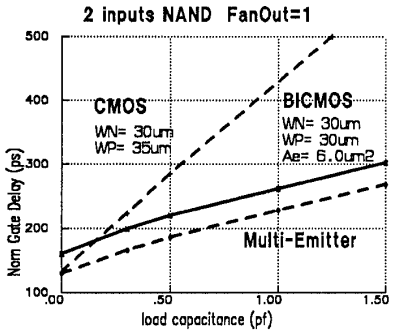


Fig 2 : 2 way NAND BICMOS : SPEED vs. LOADING

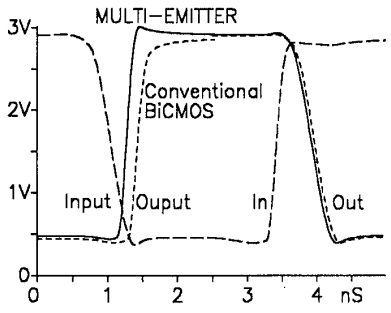


Fig 3: Typical Waveforms with BICMOS MULTI-EMITTER

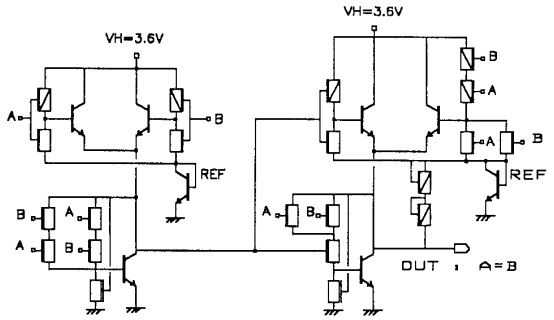


Fig 4 : 2 way XOR NOT CIRCUIT With MULTI-EMITTER

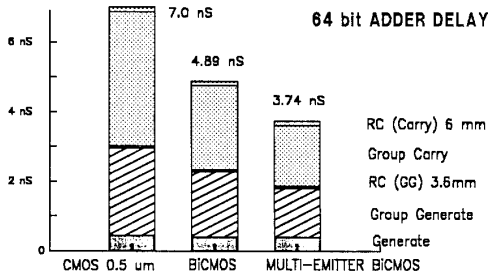


Fig 5 : PERFORMANCE of a 64 BIT ADDER with Carry Look Ahead

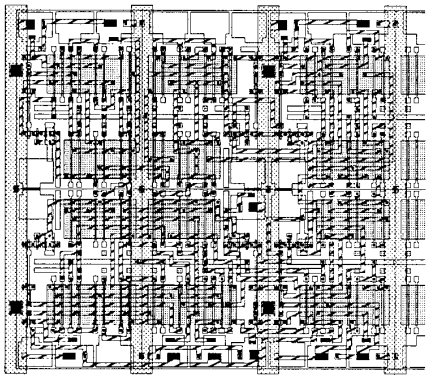


Fig 6: MULTIPLIER CELL CIRCUIT in a Gate Array structure

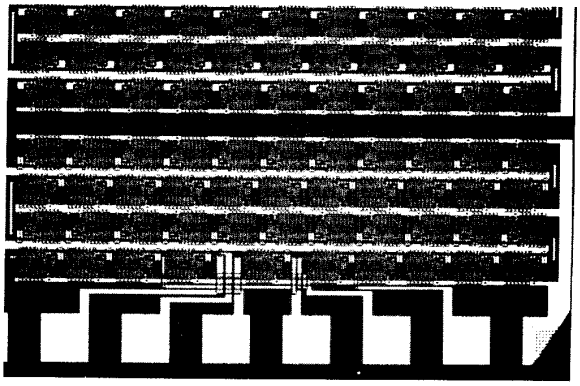


fig 7: Microphotograph of 41 stages NAND 2 BiCMOS ring oscillators