A MERGED CBi-CMOS GATE ARRAY WITH EMITTER FOLLOWER BUFFERS

Gerard Boudon, Seiki Ogura (*), Pascal Tannhof, Frank Wallart, Pierre Mollier, Jean Paul Nuez, D. Omet
Rene Cullet, Dominique Plassat, Robert Trauet, Daniel Mauchauffee

IBM France Component Development Laboratory
91102 Corbeil-Essonnes , France
(*) IBM East Fishkil, New York 12533 USA

ABSTRACT :
A new Merged Complementary Emitter Follower BiCMOS (C-EF-BiCMOS) circuit with a double Darlington diode, permits the use of FETs below a quarter of micron, while keeping 3.6V power supply. A loaded speed of 180ps is possible with leff = 0.35um in one of the simplest BiCMOS technology. A complete circuit family implemented in a gate array structure with very high density of integration due to common diffusions between the bipolars NPN/ PNP and the FET devices, is described.

- INTRODUCTION The Complementary Emitter Follower BiCMOS (C-EF-BiCMOS) circuit with NPN and vertical grounded PNP has demonstrated that it is one of the best candidate for the scaling down of the FET channel lengths to deep submicron dimensions with a reduced power supply. A new 3.6V BiCMOS circuit with FETs under 2.1V designed in a high density gate array, is proposed, achieving the fastest possible speed of such type of circuit.

- TECHNOLOGY

The complementary BiCMOS circuits are built in a technology derived from a CMOS base [1]. Since the NPNs are always tied to Vdd and PNPs tied to GND in the circuits, a minimum amount of extra process complexity is required to define N and P type subcollectors, bipolar bases, and Emitter opening. With this type of circuit, the performance is mainly dependent on the FETs and the parasitic capacitances, allowing Bipolars with low cut off frequencies (17 GHz NPN and a 7 Ghz PNP). Emitters of the NPN and the PNP are made with N+ or P+ polysilicon layers, also used as FET gate electrodes allowing 2 NFET and 2 PFET threshold voltages (Fig 1).

The PFETs and the NPN are integrated in the same N-Well, while the NFETs are integrated with the PNPs without extra isolation, to reduce parasitic capacitances. This is possible with a collector resistance low enough to avoid Latch-Up.

The target for the channel length of the FET devices was 0.5 um, while hardware has been measured with 0.55um and 0.6um for the NFET and the PFET respectively.

- OPTIMIZING CIRCUIT PERFORMANCE

The performance of a Complementary Emitter Follower BiCMOS circuit is usually limited by a dead zone operation during transients with no bipolar transistor conducting.

Such circuit can be built without offset voltage between the base of the NPN and the base of the PNP or with a NFET /PFET diode (fig 2a) or with one PN junction diode in series with a resistor or with 2 PN diodes. Problems of cross over current, latch up, poor density, results in a non competitive circuit.

The delay and the Power dissipation vary according to figure 3, with the offset voltage between the bases of the 2 bipolar transistors. Above the ideal offset of 2 Vbe's = 1.5V the power goes very high, while below the delay increases.

- Double diode Offset voltage

A novel structure [2] with a Darlington diode is proposed (see fig 2b). The double diode is mounted in a Darlington mode to reduce the offset just below the Vbe of an NPN plus a PNP. The current in a diode being reduced by 60mV for a decade in current, a VBE reduction of 100mV is obtained with a beta of 70. It is thus possible to adjust the offset voltage just below 2 Vbes with a very low DC current and with small NPNs.

The typical waveforms on figure 4 for the different offset voltage options show the benefit of the novel approach.

- low CCS

The delay of the C-EF-BiCMOS circuit depends mainly on the total capacitance on the base nodes of the bipolar transistors with in particular the Diode Collector to Substrate Capacitance (CCS) (fig 5). With the Darlington double diode a lower CCS is obtained if the collector of the top NPN is tied to Vdd with now only one isolated NPN device (connection (2) figure 2b). However the E-C voltage is higher, and the NPNs must be totally free of Pipes to avoid parasitic currents resulting in a circuit fail.

- Performance comparisons

With half micron FETs the power supply cannot exceed 3.6V without problems of voltage stress. With this technology, a conventional BiCMOS circuit with 30 um width NFET /PFETs and NPNs only, has a typical gate delay of 225ps, Fig 4.

The speed of the C-EF-BiCMOS would be slightly slower (240ps) with the same channel length (Leff= 0.45um). But the channel length can be reduced to 0.35um with the same electrical field, thus decreasing the delay down to 180ps.

The use of a reduced voltage swing gives also a power dissipation advantage for the proposed C-EF-BiCMOS circuit as a better balanced rising and falling transitions, and less dI/dt noise from gate switching than in conventional BiCMOS.

- CIRCUIT FAMILY

With the complementary BiCMOS approach a complete logic circuit family is built using 15um FETs for the logic function followed by a buffer stage made with NPNs and PNPs. To design the LSSD polarity hold shift registers, a pair of small FETs have been included in the gate array structure.

- Buffer for ECL Circuits The use of the Darlington double diode voltage shifter can be extended very efficiently in the output buffer of an ECL circuit or a NTL [3] (Non Threshold Logic) to improve circuit delay if PNPs are available.

- GATE ARRAY :

A gate array is proposed with very high density since the circuit structure is as regular as in traditional CMOS. The number of main elements (4 NFET, 4 PFET , 1 NPN, 1 PNP) in the gate array cell (fig 8) has been optimized by software. It takes into account the occurrence of each type of circuits such as NOR's NAND's XOR's etc.. in a VLSI chip. The number of elements to built each basic circuit of the library is then concatenated with the circuit occurrence to get the densest chip size. The choice here is a number of elements which permits to build an inverter , or a "NOR 2" or a "NAND 2" in one cell.

The gate array density is similar to conventional CMOS with smaller input FETs resulting in a lower input capacitance.

The wiring of the circuits is made at the first level of metal horizontally, with the help of local interconnection on a polycide level. Only the output connection between the 2 Emitters is built at the second level of metal. A small DC current is necessary to get a constant 2 Vbe offset voltage. The use of high Vt NFET's and PFET's (P and N poly gate respectively) permits to limit this current with very small devices.

REFERENCES:

[1] S.Ogura et al. "Merged Complementary BiCMOS for logic applications" 1990 VLSI technology symposium june 1990.

[2] G.Boudon P.Mollier P.Tannohf S.Ogura F.Wallart D.Omet "Improvements to complementary emitter follower drivers" patent 89480046.5

[3] C.T Chuang "NTL with complementary Emitter-follower driver : A high speed low power Push pull logic circuit" 1990 VLSI circuit Symposium june 1990.

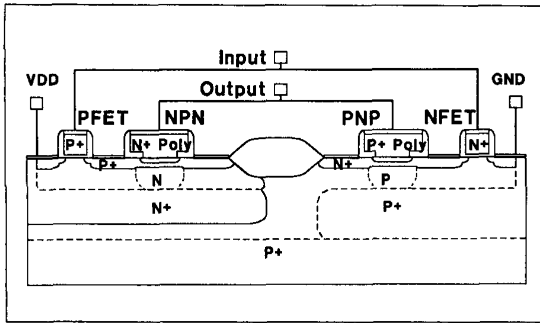

Fig 1: Merged Complementary BICMOS Cross section

- TABLE 1 -

PARAMETERS		NOMINAL VALUES
Channel Length	(NFET)	: 0.55 um
	(PFET)	: 0.60 um
Gate Oxide Thickness		: 12.0 nm
Device Vt.	(NFET)	: 0.9 Volts
	(PFET)	: -1.1 Volts
Saturation Transconductance	(NFET)	: 150 mA/V/mm
	(PFET)	: 55 mA/V/mm
N-Well Voltage		: 3.6 Volts
Substrate Voltage		: 0.0 Volts
NPN Ft		: 17 GHz
NPN Beta		: 85
PNP Ft		: 8 GHz
PNP Beta		: 20

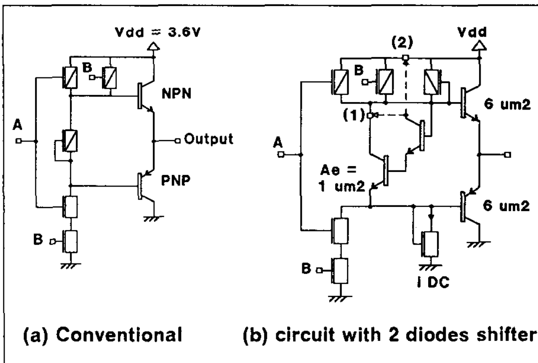

Fig 2: Complementary Emitter Follower BICMOS circuits

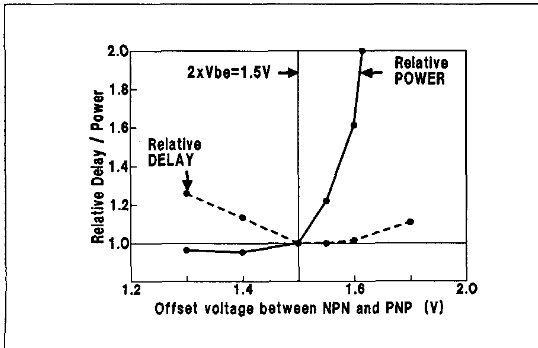

Figure 3: Power and Delay versus offset base voltage

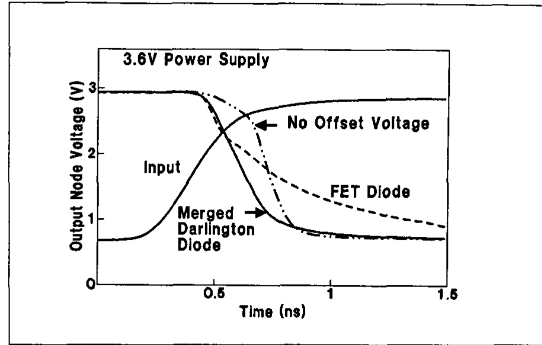

Figure 4 : Typical waveforms comparisons with BiCMOS

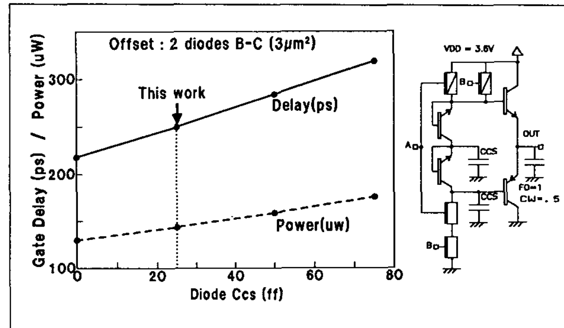

Figure 5 : NAND 2 speed and power versus diode CCS.

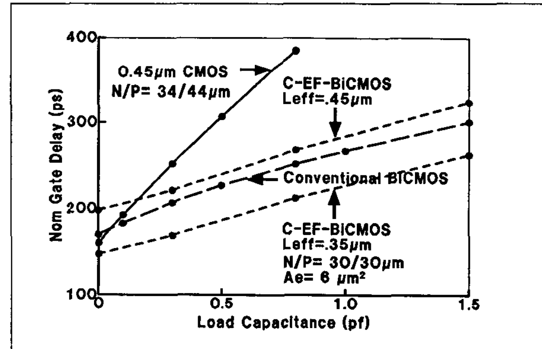

Figure 6 : 2 Input NAND BICMOS : Speed vs. Loading

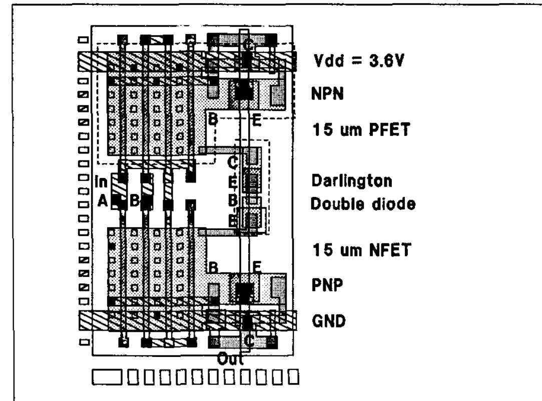

Figure 7 : NAND 2 in a 30um x48um Gate array cell