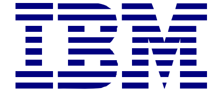
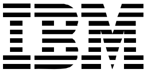
Les Processeurs PowerPC et le SOI

Gerard Boudon
IBM France



Agenda

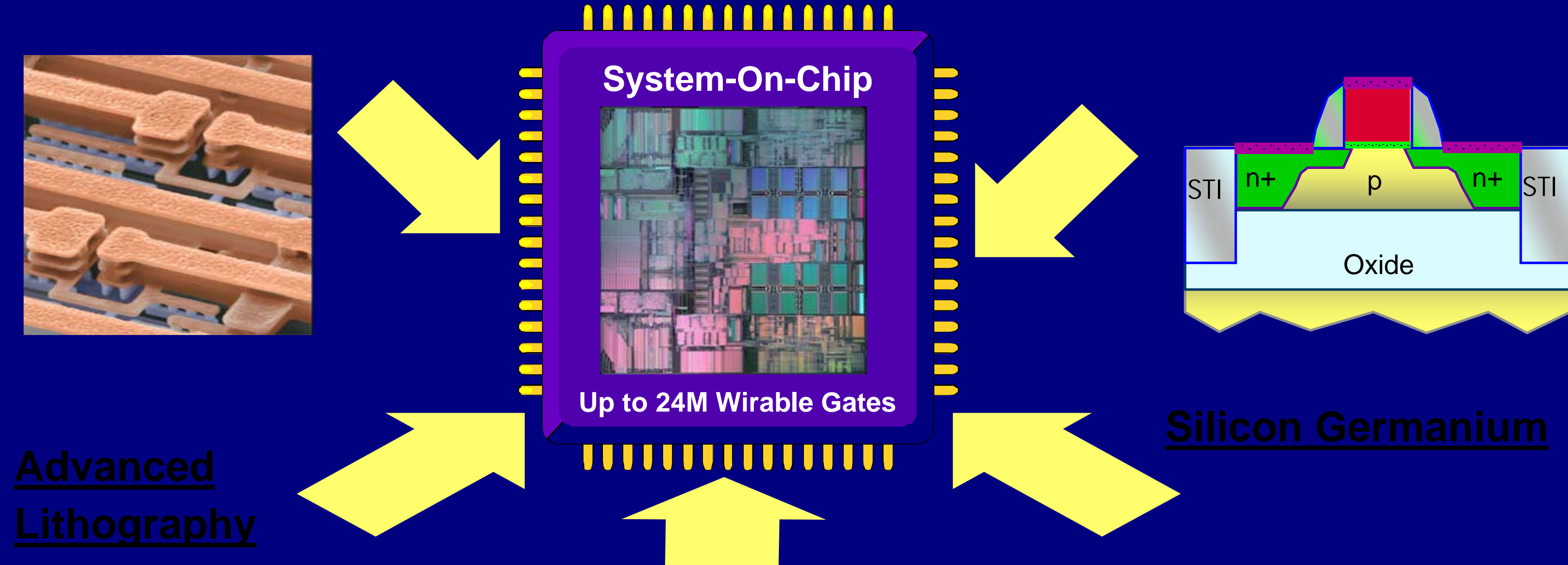


- Introduction
  - Evolution des technologies
- La technologie SOI
  - Les Avantages
  - Les Inconvenients
  - Les solutions
- Famille de PowerPC
  - PowerPC 750
  - 1GHz Power 4
- Conclusion

Key Leadership Technologies

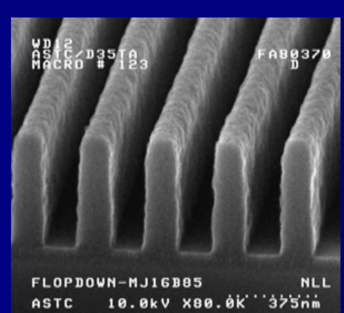
Copper Wiring

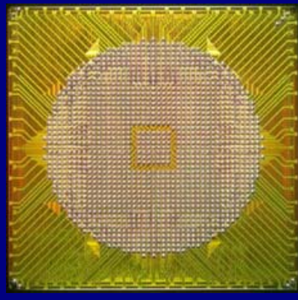
Silicon-on-Insulation



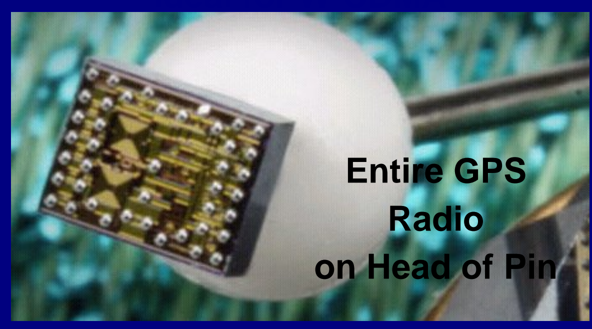
Silicon Germanium

Advanced Lithography

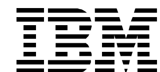




C4 Flip Chip Packaging

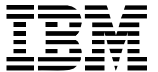


IBM Blue Logic™ Technology Roadmap

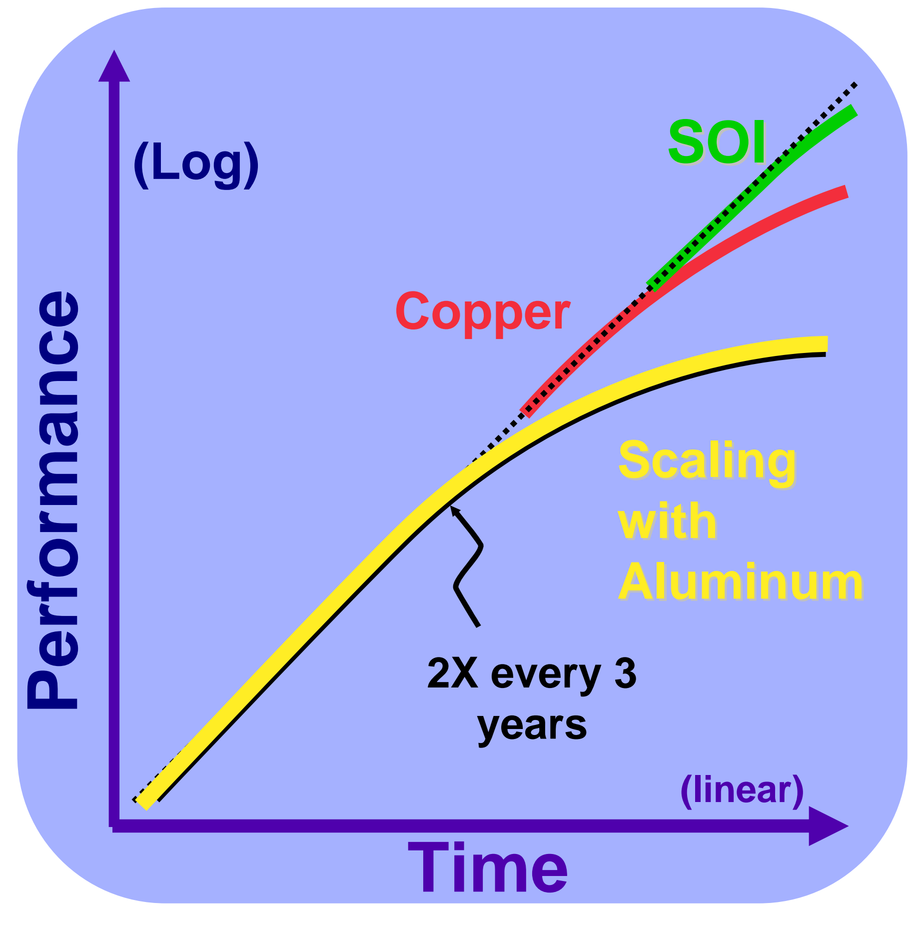


ASICS

SOI to Rescue Moore's Law



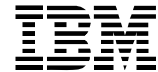
- The performance (speed) of conventional CMOS is falling behind Moore's Law.
  - aluminum wiring delays beginning to dominate.



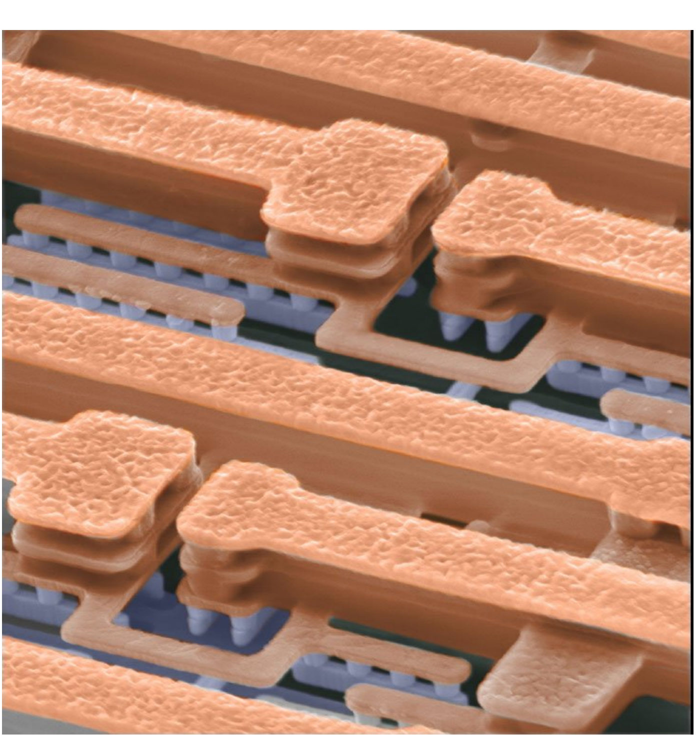
- 1997: IBM announces Copper Interconnect, enhances chip performance (speed) by 10-20%.

- 1998: IBM announces Silicon-On-Insulator (SOI), enhances chip performance (speed) by 20-35% or reduces power by 2-3x.

Copper Interconnect



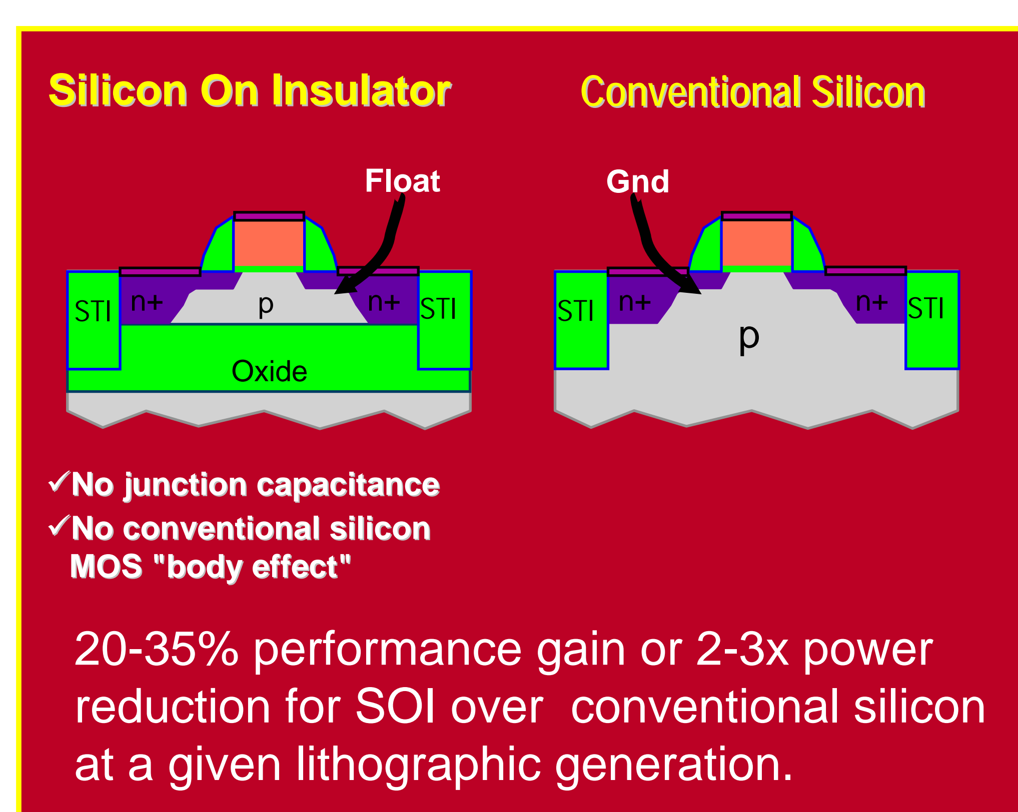
- First in industry to offer full copper wiring for chip interconnections
- Provides 10-20% performance improvement
- Best in industry density, device performance and interconnections
  - –0.16μm CMOS logic
  - –Copper improves chip performance by improving resistance and capacitance
- Volume manufacturing June 98
  - –Simple Damascene Copper processing technique
  - –Improved electromigration characteristics



Silicon On Insulator Development

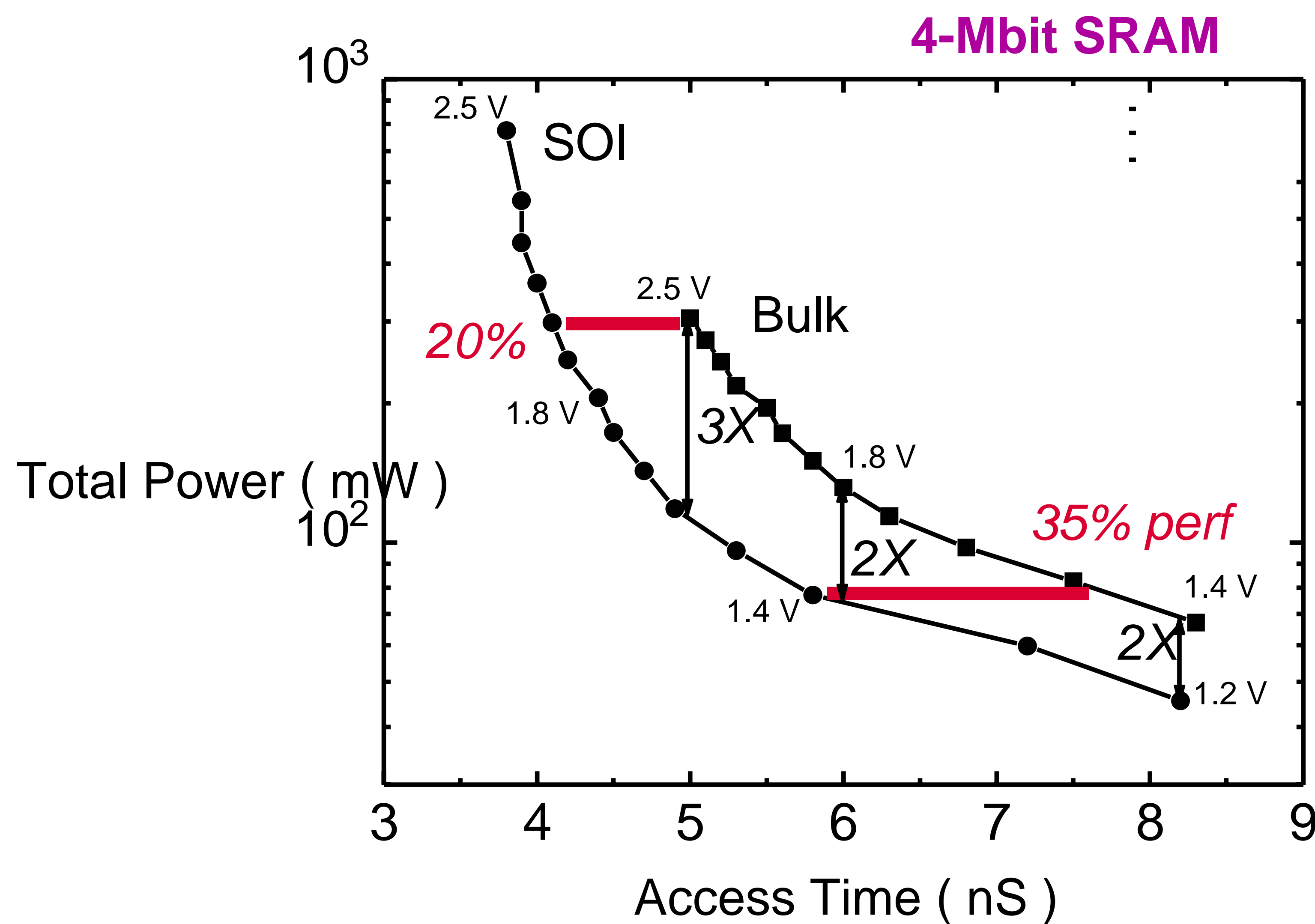
IBM has:

- Perfected Oxygen Implant & Anneal
- Achieved SOI Yields Comparable to Conventional Silicon
- Developed Partially Depleted Transistor
- Controlled Floating Body Effect
- Developed Proven Transistor Models

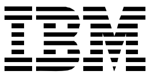


SOI Performance vs. Power Tradeoff

IBM



- 1.7-3X lower power at the same performance



SIMOX (Separation by Implantation of Oxygen) process

High dose Implant silicon with Oxygen.

Anneal the damage.

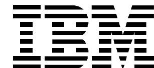
(creates an oxide layer isolating the SOI layer)

Build FET transistors.

(sub-0.25 μm CMOS process)

Same lithography and toolset as conventional bulk CMOS technologies

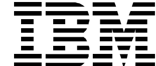
SOI : Barriers Overcome



- **Poor SOI material quality**
  - –Material supply / cost
    - ☞Perfection of SIMOX oxygen implant & anneal
    - ☞Yields comparable to bulk CMOS
- **Floating body effects**
  - –Complicated device design
  - –Unwanted effects
    - ☞Proven device models
- **Continued bulk CMOS scaling**
  - –Performance gains diminishing
    - ☞SOI demonstrates excellent performance at low voltages

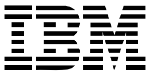
SOI Cost adder : about 10% of the processed wafer

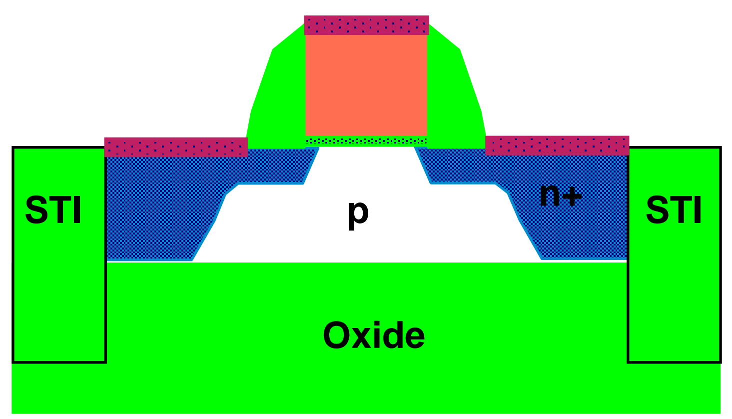
SOI : Design Concerns

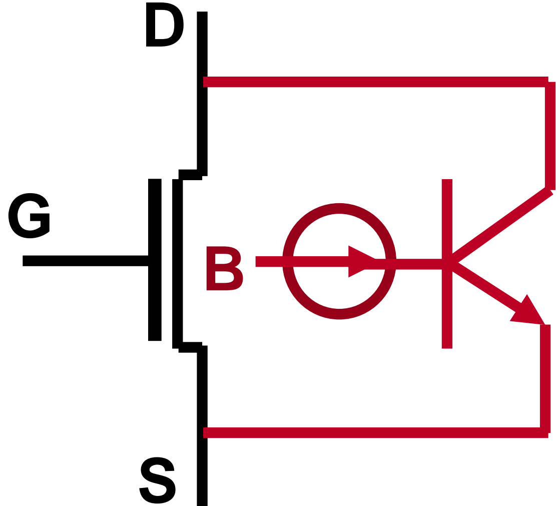


- **Floating Body Effects**
  - –Kink effect
  - –Pass-Gate leakage
  - –History dependence on delays
  - –Low device breakdown
- **Parasitic bipolar current**
- **Lower noise immunity in dynamic circuits**
- **Self heating**

SOI Device







- FET body is floating
  - V_{BS} can vary from -0.2V to VDD
    - Set by its steady state and C-Coupling
  - V_T varies as VBS change

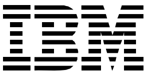
Simple Circuit Responses to Floating Body

Out
In
V_{dd}
N+ N+ P+ P+

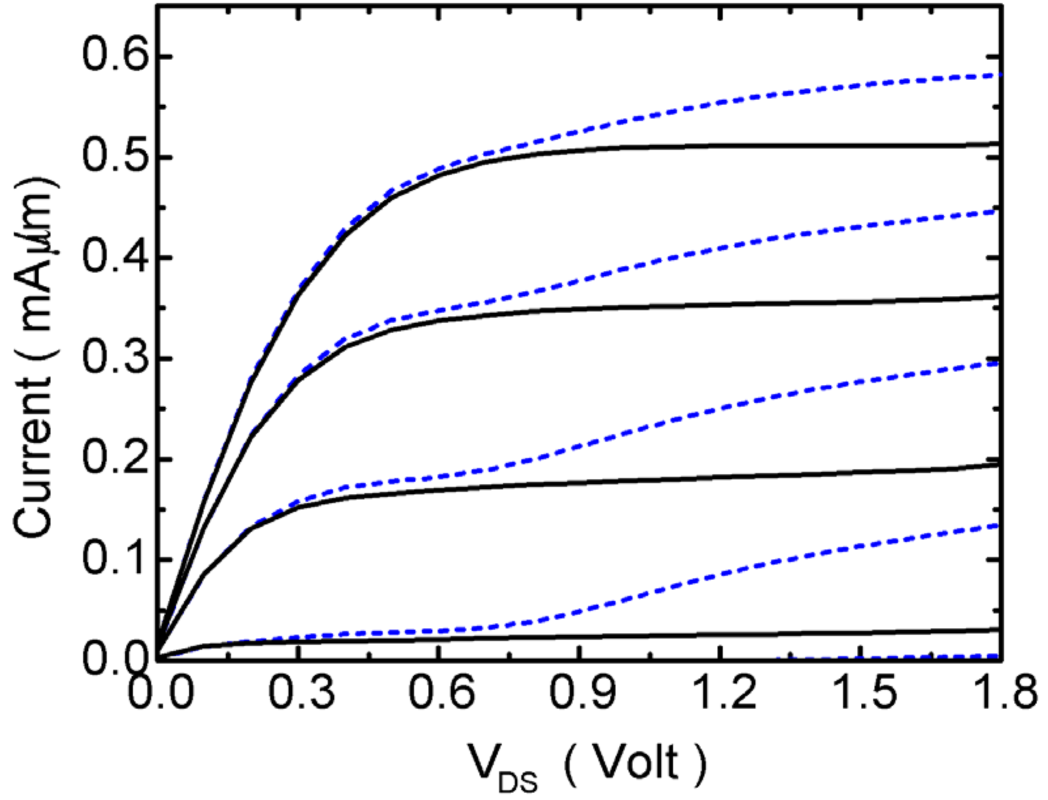
2V
PFET Body
1.43V
Out
.32V
NFET Body
0V
Fall
“Away-From”
Initial State
Rise
“Return-to”
Initial State

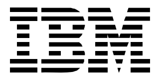
PFET
Body
2V
1.6V
NFET Body
Out
.54V
0V
Rise
“Away-From”
Initial State
Fall
“Return-to”
Initial State

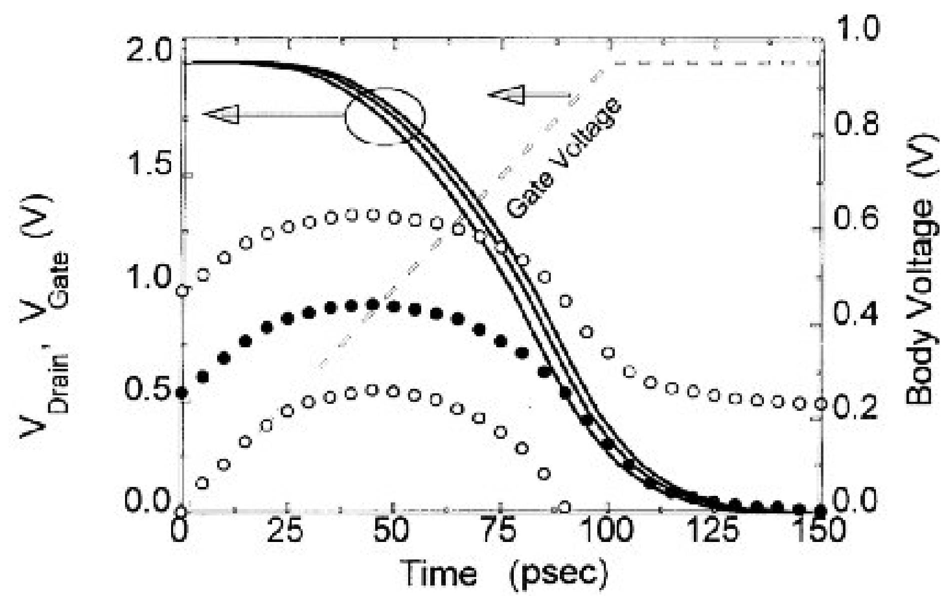
Kink Effect



- **Undesirable in analog circuits**
  - –Significant early effort to reduce the kink effect
- **IBM's approach:**
  - – Kink leads to more current in digital circuits (use partially depleted MOS)
  - –On key analog devices: Use body contact

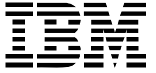


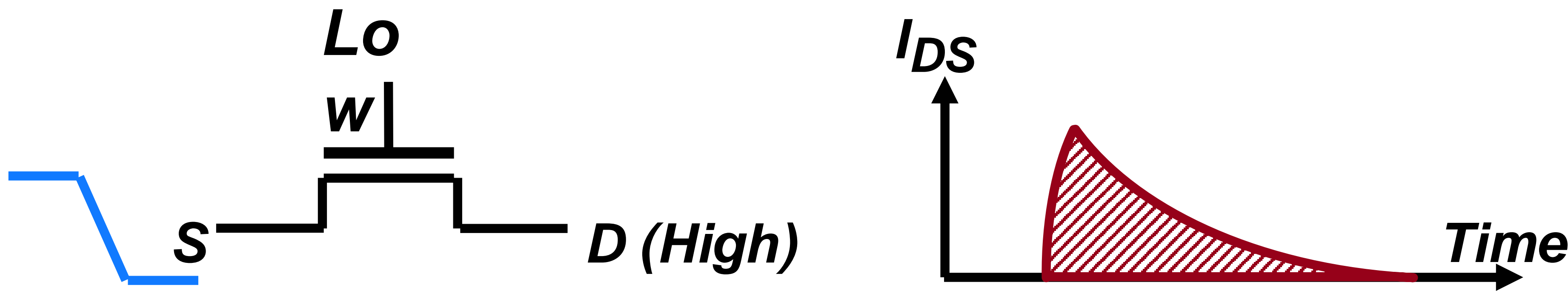




Source of Variation	Variation Delay
Across Chip Poly Variation	*15-20%*
Temperature (25-85 C)	*10-20%*
Top vs. Bottom switch in NAND	*20-35%*
VDD Variations (10%)	*10%*
"History-Dependence" Effect	***8%***

Pass-Gate leakage



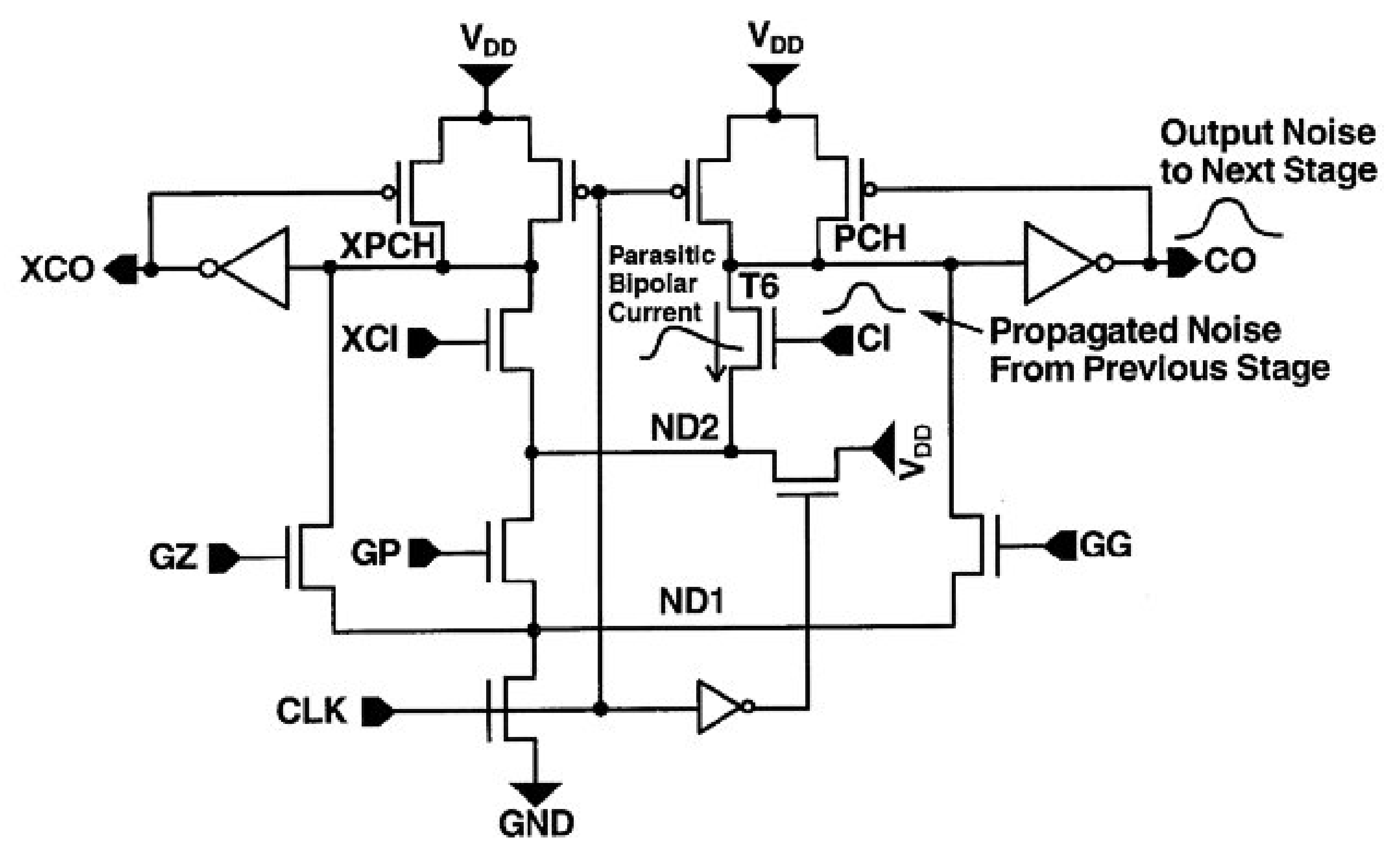


- The body of the MOS device can charge up to the supply
  - In bulk-MOS, the body is always grounded

- When the body discharges fast, a pulse of current is set through the device

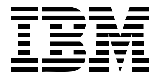
- Minimize the pass gate leakage by reducing the bipolar gain

Carry Look-Ahead Tree: Bipolar Current Sensitivity



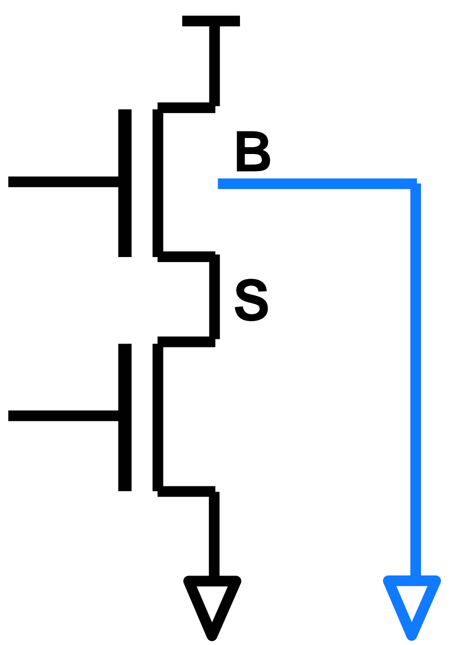
Super Position of Noise Causes Corruption after Third stage

Body Effect in CMOS SOI



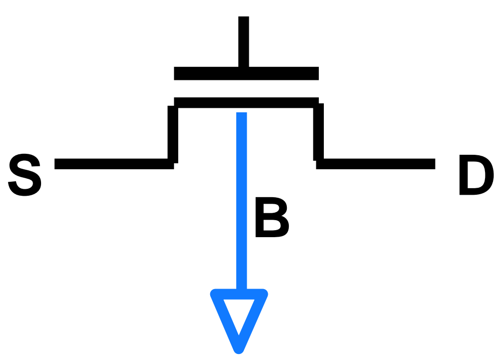
- No "MOS reverse body effect":
  - In Bulk MOS, if VBS < 0, then VT will increase
  - More current in stacked and pass-gate device
- In SOI

  VBS > 0 most of the time, (VT lowers), results in more current.
  - Optimum for low voltage (i.e. power) operation

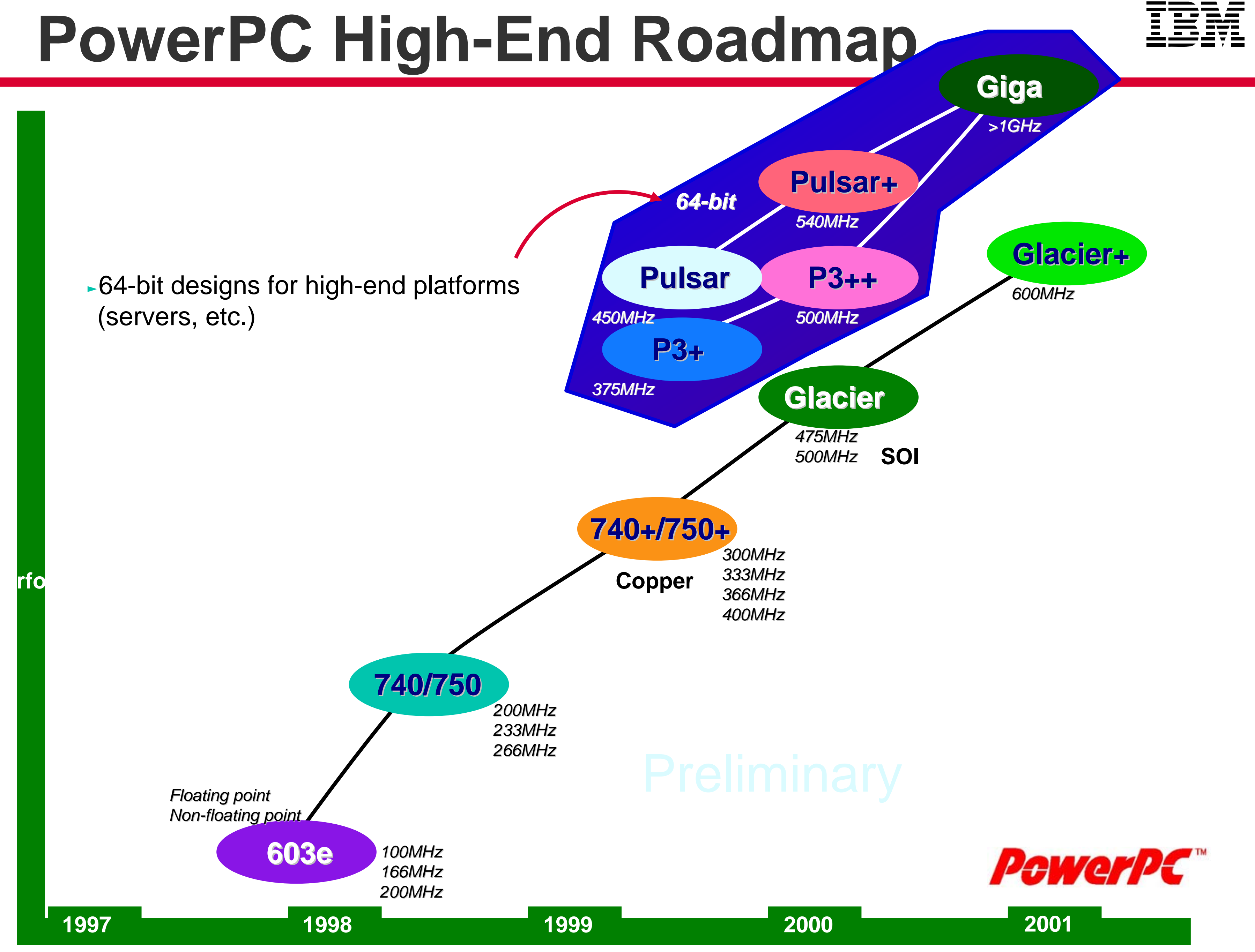


R.O. Circuit	Gain Over Bulk
Inverter	*20-25%*
2-Way NAND	*27-33%*
3-Way NAND	*40-45%*
4-Way NAND	*50-55%*

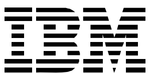
More performance gain for stacked circuits



PowerPC High-End Roadmap



PowerPC 750 implementation



Completion

Instruction Fetch

32KB Icache

Sys unit

Dispatch

Branch Unit

FXU 1

FXU 2

GPR

Renames

Load Store Unit

FPR

Renames

FPU

32KB Dcache

L2 tags

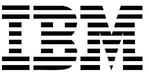
L2 Interface

60X Bus

SRAM

System Bus

PowerPC 750 with SOI



Copper Metal

Tungsten Via

Tungsten Local Interconnect

Device Layer 0.18um

Buried Oxide 0.4 um

Enhanced and colorized SEM view of SOI device in cross-section with wiring and SOI chip image superimposed.

copyright IBM 1998

Metal Wiring

Transistor

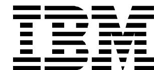
SOI

Oxide Insulator

Silicon Wafer

IBM

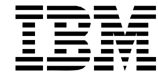
580MHz RISCMicroprocessor in S0I



PowerPC 750 with SOI

- 32-Bit PowerPC Architecture
- 32-KB Data and 32-KB Instruction Cache
- Integrated L2 Cache Controller
- L2 Cache Sizes of 256KB, 512KB or 1MB
- Two Instructions Dispatched per Cycle
- 25 SPECint95 and 14.5 SPECfp95 at 580 MHz(estimated)
- A 40mm* Commercial 32b RISC Microprocessor has been Successfully Implemented in a:
  - 0.1 2um Leff - Partially Depleted SOI Process
- A Speed Advantage of 20% Has Been Demonstrated

Ref : ISSCC99 Feb 99

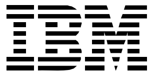


- **Partially Depleted SOI Devices Can Achieve Performance Gains of up to 35%**

  - **10x Reduction in Source/Drain Capacitance Results in a 12%Performance Advantage**

  - **Reduction of Source-to-Body Reverse Bias Accounts for Another 15-25% Improvement Depending on Circuit Topology**

Bulk vs SOI Critical-Path Comparison



Standard Cell

Bulk

Custom

Interconnect

SOI

Custom

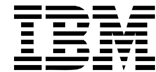
Relaxed Custom
(Self timed dynamic circuit)

0 500 1000 1500 2000 2500

Delay (ps)

Ref : ISSCC99 Feb 99

Power4 : 1GHz dual CPU Chip



- Single MCM
  with 8 Processors
- 64 bit RISC
- 5 Instr issue/cycle
- Dynamic scheduling

L2 Cache about 1.5MB

Power: 125 W (est.)

Application:
- High End Servers

CPU1 1GHz
CPU2 1GHz
100 GB/s
L2 Cache
L3 Dir
Chip-Chip Communication
333MHz
10 GB/s
Memory
L3
Expansion Bus
500MHz
35 GB/s
4 Chips MCM

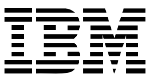
Ref : Microprocessor Forum Oct 99

POWER4 Leverages IBM Technologies

- **Process**
  - –IBM CMOS 8S2, 0.18um
  - –Copper and SOI with 7 layers of metal
  - –170 million transistors
- **Package**
  - –Uses large number of I/Os at chip and MCM level
  - – >2,200 I/O with >5,500 Pins
  - – Multi Chip Module (MCM) for dense integration
  - – High bandwidth with fast busses
  - – Elastic I/O provides >500 MHz chip-chip busses

Ref : Microprocessor Forum Oct 99

POWER4 the Gigahertz processor



Technology
- 400mm2
- 170M tx
- CMOS 0.18um
- SOI
- 7 layer Metal

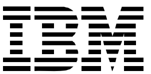
Architecture

Two > 1GHz superscalar processor

FPU ISU FXU FXU ISU FPU
IDU IDU
IFU BXU LSU LSU IFU BXU
L3 Directory and Control
L2 L2 L2

Ref : Microprocessor Forum Oct 99

Conclusion



- Partially-Depleted Silicon on Insulator (SOI) results in 20-35% performance gain over comparable bulk technology.
- Static circuit convert with no change
- Some challenge in dynamic circuits & SRAM
- Demonstration in several PowerPC Processors
  - PowerPC 750
  - 1 GHz Power4

Key Leadership Technologies

Copper Wiring

Silicon-on-Insulation

System-On-Chip

Up to 24M Wirable Gates

Silicon Germanium

Advanced Lithography

C4 Flip Chip Packaging